IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Paul, et al.	
Application No.: 10/813,589	Group Art Unit: 2817
Filed: 3/30/2004	Examiner: SHINGLETON, MICHAEL B
Title: POWER AMPLIFIER CIRCUITRY AND METHOD	Attorney Docket No.: SIL.P0078

SECTION 1.131 DECLARATION OF BRUCE A. JOHNSON

I, Bruce A. Johnson, hereby declare the following:

1. I am the attorney of record of patent application Serial Number 10/813,589, filed on 3/30/2004, which is a continuation of co-pending commonly owned US patent application number 10/390,935 filed on March 18, 2003 (US Patent 6,788,141), entitled "Power Amplifier Circuitry And Method", which is a continuation of US patent application number 09/660,123 filed on September 12, 2000 (US Patent 6,549,071), entitled "Power Amplifier Circuitry And Method".

2. The Examiner has cited Mandelman et al., US Patent 6,355,531, issued on March 12, 2002, and filed on August 9, 2000.

3. I am the attorney that prepared parent patent application Serial Number 09/660,123 filed on September 12, 2000.

4. The inventors were in possession of the subject matter of the invention set forth in the patent applications listed in paragraph 1 earlier than the August 9, 2000 filing date of Mandelman et al. Attached as evidence is a copy of 2 pages of an invention disclosure document that I received by facsimile from inventor Timothy Dupuis describing the subject matter at question. The disclosure is signed and dated by inventor Timothy Dupuis. The dates on the disclosure document are prior to August 9, 2000. The dates on the disclosure document are redacted, but the facsmily transmission data is not, which indicates a transmission date of December 7, 1999.

5. From the time prior to August 9, 2000 to the filing date of September 12, 2000 (approximately 23 working days), I was working dilligently with the inventors to complete the patent application that was filed on September 12, 2000 and assigned Serial Number Number 09/660,123. This work included revising and finalizing the patent application.

6. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

4/16/08
Date

Bruce A. Johnson

[redacted] RF POWER AMPLIFIER

Possible Patentable Ideas

(1) Basic Architecture - NMOS only output w. direct drive

(2) The use of .5um and .35um gate length (actually different oxide thickness devices), to provide a RF power amplifier.

Digital CMOS processes at sub-micron design rules (.35um - .25um) typically provide a high breakdown device (.5um) as an option. This is used to provide 5V drive capability in digital systems.

This architecture makes use of this device in the driver. The short channel devices are required in the pre-driver circuitry dve to their high FT and they do not see high voltages (0 → VDD) only. The high breakdown devices are used for M1, M2, M3 and M4. M1, M2 and M3 can see a Vgd of 2·VDD in this architecture. With VDD = 3V a breakdown of 6V is required. This can be achieved with the .5um devices.

(3) The use of M5 to start-up the network. This is not fully developed. M5 is used to help provide a return current for the L1, M1 loop during startup — I'll describe in more detail if this continues to look promising.

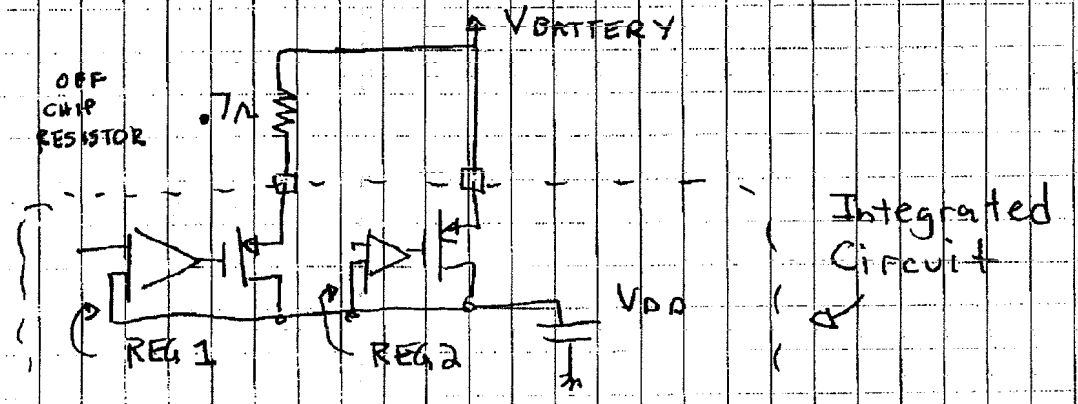
(4) The use of an 'on chip' bypass capacitor C2. This is required since with the CMOS push-pull scheme any series inductance with this capacitor is a big problem. It also simplifies the PCB design in that only a "large" inductor is needed to VBATTERY.

(5) The ON-CHIP VOLTAGE REGULATOR

During battery charge up the battery voltage can get much higher than the steady-state voltage. Applying this voltage directly to a CMOS P.A. could cause breakdown problems.

When the battery is being charged or during it's initial use after charge P.A. efficiency is not important and a linear regulator can be used to drop this voltage to one the chip can handle is used.

When the battery is high and P.A. is transmitting at maximum power there is a high power dissipation in the linear regulator that could exceed the package power rating (especially for GPRS systems). To assist in this problem an off-chip resistor can be used. The final regulator is as follows:



A control circuit will use REG. 1 to provide as much power as it can before enabling REG. 2 to provide the difference (more on this later). This will move some of the power to the off-chip resistor.

[redacted]